

WHAT IS CLAIMED IS:

1 1. A reconfigurable chip comprising:
2 a multiplication block including at least one multiplication unit and a
3 group of selectable adder units operably connected to the multiplication unit,
4 wherein the adder units are selectively connectable in different configurations; and
5 interconnect elements operably connected to the multiplication block, the
6 interconnect elements adapted to selectively connect together the multiplication
7 block with other reconfigurable units.

1 2. The reconfigurable chip of Claim 1 wherein the multiplication
2 block further comprises input multiplication multiplexers for the block.

1 3. The reconfigurable chip of Claim 2, wherein there are fewer
2 block input multiplexers than input multiplexers for the multiplication units.

1 4. The reconfigurable chip of Claim 1 wherein the adder units
2 include input multiplexers.

1 5. The reconfigurable chip of Claim 1 wherein the multiplication
2 units include input multiplexers.

1 6. The reconfigurable chip of Claim 1 wherein there are multiple
2 multiplication units in each block.

1 7. The reconfigurable chip of Claim 1 wherein the instruction
2 configures the multiplexers in the multiplication block.

1 8. The reconfigurable chip of Claim 1 wherein the multiplication
2 block includes registers associated with the multiplication unit and adder units.

1 9. The reconfigurable chip of Claim 1 wherein the other type of unit
2 is operably connectable to the adder units and can be used instead of multiplier
3 units.

1 10. The reconfigurable chip of Claim 9 wherein the other type of unit
2 comprises the despreader/correlator unit.

1 11. The reconfigurable chip of Claim 1 wherein the adder units can
2 be connected together into chains.

1 12. The reconfigurable chip of Claim 1 wherein the interconnect
2 elements are adapted to transfer word length data.

1 13. The reconfigurable chip of Claim 1 wherein further comprising an
2 instruction memory storing multiple instructions for the reconfigurable functional
3 units.

1 14. The reconfigurable chip of Claim 13 wherein a state machine
2 addresses the instruction memory.

1 15. The reconfigurable chip of Claim 1 wherein the multiplication
2 block includes a selectable output register for the multiplier units and the adder
3 units.

1 16. The reconfigurable chip of Claim 1 wherein the multiplication
2 block includes at least two multiplication units.

1 17. The reconfigurable chip of Claim 1 wherein the multiplication
2 block includes at least four multiplication units.

1 18. A reconfigurable chip including:
2 a multiplication block including at least one input multiplexer, a
3 multiplication unit operably connected to the input multiplexer, a group of
4 selectable adder units operably connected to the multiplication unit, wherein the
5 adder units are selectively connectable in different manners; and
6 an instruction memory storing multiple instructions for the multiplication
7 block.

1 19. The reconfigurable chip of Claim 18 wherein there are input
2 multiplexers for the block.

1 20. The reconfigurable chip of Claim 18 wherein there are input
2 multiplexers associated with the adder units.

1 21. The reconfigurable chip of Claim 18 wherein there are input
2 multiplexers for the multiplication unit.

1 22. The reconfigurable chip of Claim 18 wherein there are fewer
2 block input multiplexers and then input multiplexers for the multiplication units.

1 23. The reconfigurable chip of Claim 18 wherein there are multiple
2 multiplication units in each block.

1 24. The reconfigurable chip of Claim 23, wherein there are at least
2 four multiplication units in each multiplication block.

1 25. The reconfigurable chip of Claim 18 wherein the multiplication
2 block includes a decoder to decode a portion of the instruction.

1 26. The reconfigurable chip of Claim of 18 wherein the multiplication
2 block includes registers associated with the adders units and multiplication units.

1 27. The reconfigurable chip of Claim 26 wherein the registers of
2 selectable output registers.

1 28. The reconfigurable chip of Claim 18 wherein another type of unit
2 is operably connectable to the adders and can be used instead of the multiplier unit.

1 29. The reconfigurable chip of Claim 28 wherein the other type of
2 unit is a despreader/correlator unit.

1 30. The reconfigurable chip of Claim 18 wherein the adder units can
2 be connectable into a chains.

1 31. The reconfigurable chip of Claim 18 further comprising
2 interconnect units operably connected to the multiplication block.

1 32. The system of Claim 18 wherein the instruction memory is
2 addressed by a state machine.

1 33. A reconfigurable chip including:
2 a multiplication block including at least one input multiplexer, a
3 multiplication unit operably connected to the input multiplexer, a group of
4 selectable adder units operably connected to the multiplication unit, wherein the
5 adder units are selectively connectable in different manners; and
6 an instruction memory storing multiple instructions for the multiplication
7 block.

1 34. The multiplication block of Claim 33 wherein there are fewer
2 block input multiplexers than input multiplexers for the multiplication units.

1 35. The multiplication block of Claim 33 wherein there are at least
2 four multiplication units in each multiplication block.

1 36. The reconfigurable chip of Claim 33, wherein there are four
2 multiplication units in each multiplication block.

1 37. The reconfigurable chip of Claim 33 wherein the multiplication
2 blocks are configured by an instruction.

1 38. The reconfigurable chip of Claim 37 wherein at least portions of
2 the instruction is sent to a decoder in the multiplication block.

1 39. The system of Claim 33 wherein the multiplication block includes
2 registers in the multiplication block to store output values.

1 40. The multiplication block of Claim 39 wherein the registers are
2 selectable output registers.

1 41. The multiplication block of Claim 33 wherein there is another
2 type of unit operably connected to the adder units strictly used instead of the
3 multiplier unit.

1 42. The system of Claim 40 wherein the other type of unit comprises
2 a despreader/correlator unit.

1 43. The multiplication unit block of Claim 33 wherein the adder units
2 can be arranged into a chain.

1 44. The multiplication block of Claim 33 further associated with
2 interconnect elements adapted to transfer data between the multiplication block and
3 other local elements.

1 45. The multiplication block of Claim 33 further including an
2 instruction memory storing multiple instructions for the reconfigurable functional
3 units.

1 46. The multiplication block of Claim 45 further comprising a state
2 machine addressing the instruction memory.

1 47. A multiplication block on a reconfigurable chip, the multiplication
2 block including:
3 multiple block input multiplexers;
4 at least two multiplication units, each multiplication unit associated with
5 two multiplication input multiplexers, the multiplication input multiplexers
6 operably connected to the multiple block input multiplexers; and

7 a group of selectable adder units with associated adder input
8 multiplexers, the adder input multiplexers operably connected to the multiplication
9 units.

1 48. A reconfigurable chip comprising:
2 a multiplication block including at least one multiplication unit and a
3 group of selectable adder units operably connected to the multiplication unit,
4 wherein the adder units are selectively connectable in different configurations; and
5 reconfigurable functional units operably connectable to the multiplication
6 block, the reconfigurable functional units including an arithmetic logic unit and a
7 shifter unit units.